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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,073	08/06/2003	Douglas Gene Keithley	10021152-1	7215

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EXAMINER	
FAULK, DEVONA E	

ART UNIT	PAPER NUMBER
2615	

NOTIFICATION DATE	DELIVERY MODE
09/13/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/635,073	KEITHLEY, DOUGLAS GENE	
	Examiner	Art Unit	
	Devona E. Faulk	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/6/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 6/22/2007 have been fully considered but they are not persuasive.

The applicant essentially asserts that Lavaud fails to explicitly disclose generating a modulated square-wave signal that is on when both the square wave signal and the modulation signal are on and off when one or both of the square-wave of the square-wave signal and the modulation signal are off. The examiner disagrees. Lavaud discloses an AND gate adapted to combine, in a logical AND, operation, the audio frequency square-wave signal with the modulation signal (AND gate labeled G1; Figure 2) producing a modulated square-wave signal through AND gate. It is known in the art that the truth table for an AND gate is

Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

With 1=on and 0=off. It is implicit then that the modulated square-wave signal is on when both the square-wave signal and the modulation signal are on and off when one or both of the square-wave signal and the modulation signal is off.

2. Claim 12 is cancelled.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Lavaud (US 5,189,705).

Regarding claim 7, Lavaud discloses a method of generating a modulated square-wave audio signal (Figure 2; column 1,line 64-column 2, line 23), the method comprising:

generating a square-wave audio signal having a first audio frequency (pulse I; Figure 2; column 1, line 64-column 2, line 5);

repeatedly counting a predetermined range of values generating count signals (up/down counter; Figure 2; column 2, lines 1-6);

modulating the count signal with a volume control signal resulting in a modulation signal (Figure 2; column 2, lines 16-27); and

modulating the square-wave audio signal with the modulation signal to generate a modulated square-wave signal that is on when both the square wave signal and the modulation signal are on and off when one or both of the square-wave of the square-wave signal and the modulation signal are off (Lavaud discloses an AND gate adapted to combine, in a logical AND, operation, the audio frequency square-wave signal with

the modulation signal (AND gate labeled G1; Figure 2) producing a modulated square-wave signal through AND gate. It is known in the art that the truth table for an AND gate is

Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

With 1=on and 0=off. It is implicit then that the modulated square-wave signal is on when both the square-wave signal and the modulation signal are on and off when one or both of the square-wave signal and the modulation signal is off (Figure 2; column 2, lines 16-30).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavaud (US 5,189,705) in view of Eddington et al. (US 5,165,017).

Regarding claim 1, Lavaud discloses

a square-wave audio signal generator adapted to generate square-wave signal at an audio frequency (pulse I; Figure 2; column 1, line 64-column 2, line 5) ;

a counter adapted to digitally count from zero to a predetermined number (up/down counter; Figure 2; column 2, lines 1-6);

a register adapted to hold a volume control value (MEM, Figure 2; column 2, lines 8-11);

a comparator connected to said counter and connected to said register, said comparator adapted to compare a present count from the counter with the volume control value and produce a modulation signal (CMP,Figure 2; column 2, lines 16-27); and

an AND gate connected to said square-wave audio signal generator and connected to said comparator, said AND gate adapted to combine, in a logical AND, operation, the square-wave signal with the modulation signal to generate a modulated square-wave signal that is on when both the square wave signal and the modulation signal are on and off when one or both of the square-wave of the square-wave signal and the modulation signal are off (Lavaud discloses an AND gate adapted to combine, in a logical AND, operation, the audio frequency square-wave signal with the modulation signal (AND gate labeled G1; Figure 2) producing a modulated square-wave signal through AND gate. It is known in the art that the truth table for an AND gate is

Input A	Input B	Output Q

0	0	0
0	1	0
1	0	0
1	1	1

With 1=on and 0=off. It is implicit then that the modulated square-wave signal is on when both the square-wave signal and the modulation signal are on and off when one or both of the square-wave signal and the modulation signal is off (Figure 2; column 2, lines 16-30;AND gate labeled G1; Figure 2).

Lavaud fails to disclose that these elements are on an IC chip. The concept of an IC chip having a plurality of elements is known in the art as taught by Eddington (90 integrated chip, Figure 1; column 8, lines 23-55). It would have been obvious to modify Lavaud by including all the elements on an integrated circuit chip in order to make sure the electronic elements are secure.

Regarding claim 6, Lavaud as modified by Eddington discloses wherein the integrated circuit is an application specific integrated circuit chip (ASIC) (Eddington/s chip is application specific).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lavaud (US 5,189,705) as applied above to claim 1 and Eddington et al. (US 5,165,017) as applied above to claim 1 in further view of Welch (US 3,932,849).

Regarding claim 2, Lavaud as modified by Eddington fails to disclose that the frequency of the square wave audio signal generator is within a range from 500 Hz to five KHz. Welch discloses a square-wave generator having a frequency of

500 Hz (column 2, lines 35-37). It would have been obvious to modify Lavaud as modified by Eddington so that the frequency of the square-wave generator is 500 Hz in order to provide a square-wave generator having a frequency that is within a desired range as chosen by the designer to meet a design specification.

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavaud (US 5,189,705) as applied above to claim 1 and Eddington et al. (US 5,165,017) as applied above to claim 1 in further view of Nakamura (US 4,724,493).

Regarding claims 3 and 4, Lavaud as modified by Eddington fails to disclose that the counter is a 5-bit counter with a counter frequency on the order of MHz. Nakamura discloses a 5-bit counter having a counter frequency on the order of MHz (column 3, lines 52-54). It would have been obvious to modify Lavaud as modified by Eddington so that the counter is a 5-bit counter with a counter frequency on the order of MHz as desired in order to provide a counter that meets design specifications.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lavaud (US 5,189,705) as applied above to claim 1 and Eddington et al. (US 5,165,017) as applied above to claim 1 in view of Tanikawa et al. (US 2002/0048193)..

Regarding claim 5, Lavaud as modified by Eddington fails to disclose that the register is a pulse width register having five bits. Tanikawa discloses a register the controls a pulse width (page 7, paragraph 0083; reads on pulse width register). The examiner takes official notice that the bit size of a register is known to be variable

depending upon how many bits the designer want it to have. It would have been obvious to modify Lavaud as modified by Eddington so that the register is a pulse width register in order to provide better control over the device.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lavaud (US 5,189,705) as applied above to claim 7 in further view of Welch (US 3,932,849).

Regarding claim 8, Lavaud fails to disclose that the frequency of the square wave audio signal generator is within a range from 500 Hz to five KHz. Welch discloses a square-wave generator having a frequency of 500 Hz (column 2, lines 35-37). It would have been obvious to modify Lavaud so that the frequency of the square-wave generator is 500 Hz in order to provide a square-wave generator having a frequency that is within a desired range as chosen by the designer to meet a design specification.

11. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavaud (US 5,189,705) as applied above to claim 7 in further view of Nakamura (US 4,724,493).

Regarding claims 9 and 10, Lavaud fails to disclose that the counter is a 5-bit counter with a counter frequency on the order of MHz. Nakamura discloses a 5-bit counter having a counter frequency on the order of MHz (column 3, lines 52-54). It would have been obvious to modify Lavaud so that the counter is a 5-bit counter with a counter frequency on the order of MHz as desired in order to provide a counter that meets design specifications.

12. Claims 13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavaud (US 5,189,705) in view of Eddington et al. (US 5,165,017) in view of the AAPA (Figures 1A and 1B).

Regarding claim 13, Lavaud discloses

an amplifier subsystem (AMP, speaker , Figure 1) adapted to amplify the signal;

a square-wave signal generator adapted to generate a square-wave signal at an audio frequency (pulse I; Figure 2; column 1, line 64-column 2, line 5) ;

a counter adapted to digitally count from zero to a predetermined number (up/down counter; Figure 2; column 2, lines 1-6);

a register adapted to hold a volume control value (MEM, Figure 2; column 2, lines 8-11);

a comparator connected to said counter and connected to said register, said comparator adapted to compare a present count from the counter with the volume control value and produce a modulation signal (CMP,Figure 2; column 2, lines 16-27); and

an AND gate connected to said square-wave audio signal generator and connected to said comparator, said AND gate adapted to combine, in a logical AND, operation, the audio frequency square-wave signal with the modulation signal to generate a modulated square-wave signal that is on when both the square wave signal and the modulation signal are on and off when one or both of the square-wave of the square-wave signal and the modulation signal are off (Lavaud discloses an AND gate adapted to combine, in a logical AND, operation, the audio frequency square-wave

signal with the modulation signal (AND gate labeled G1; Figure 2) producing a modulated square-wave signal through AND gate. It is known in the art that the truth table for an AND gate is

Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

With 1=on and 0=off. It is implicit then that the modulated square-wave signal is on when both the square-wave signal and the modulation signal are on and off when one or both of the square-wave signal and the modulation signal is off (Figure 2; column 2, lines 16-30;AND gate labeled G1; Figure 2).

Lavaud fails to disclose that these elements are on an IC chip. The concept of an IC chip having a plurality of elements is known in the art as taught by Eddington (90 integrated chip, Figure 1; column 8, lines 23-55). It would have been obvious to modify Lavaud by including all the elements on an integrated circuit chip in order to make sure the electronic elements are secure.

Lavaud as modified by Eddington fails to disclose that the amplifier subsystem is adapted to filter the modulated square-wave audio signal and to amplify the filtered audio signal and is connected to the IC chip. . The AAPA discloses an amplifier subsystem adapted to filter the modulated square-wave audio signal and to amplify the

filtered audio signal and of amplifier subsystem being connected to the chip (Figures 1A, 1B; page 3,paragraph 0006). It would have been obvious to modify Lavaud so that the amplifier subsystem is adapted to filter the modulated square-wave signal and to amplify the signal as taught by AAPA in order to provide for digital amplification.

Regarding claim 18, Lavaud as modified by Eddington and AAPA discloses wherein said amplifier subsystem comprises a resistor-capacitor (RC) filter connected to a fixed gain amplifier (AAPA, Figure 1B, page 3, paragraph 0006).

13. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lavaud (US 5,189,705) as applied above to claim 13 and Eddington et al. (US 5,165,017) as applied above to claim 13 in view of the AAPA (Figures 1A and 1B) as applied above to claim 13 in further view of Welch (US 3,932,849).

Regarding claim 14, Lavaud as modified by Eddington and AAPA fails to disclose that the frequency of the square wave audio signal generator is within a range from 500 Hz to five KHz. Welch discloses a square-wave generator having a frequency of 500 Hz (column 2, lines 35-37). It would have been obvious to modify Lavaud as modified by Eddington so that the frequency of the square-wave generator is 500 Hz in order to provide a square-wave generator having a frequency that is within a desired range as chosen by the designer to meet a design specification.

14. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavaud (US 5,189,705) as applied above to claim 13 and Eddington et al. (US

5,165,017) as applied above to claim 13 in view of the AAPA (Figures 1A and 1B) as applied above to claim 13 in further view of Nakamura (US 4,724,493).

Regarding claims 15 and 16, Lavaud as modified by Eddington and AAPA fails to disclose that the counter is a 5-bit counter with a counter frequency on the order of MHz. Nakamura discloses a 5-bit counter having a counter frequency on the order of MHz (column 3, lines 52-54). It would have been obvious to modify Lavaud as modified by Eddington so that the counter is a 5-bit counter with a counter frequency on the order of MHz as desired in order to provide a counter that meets design specifications.

15. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lavaud (US 5,189,705) as applied above to claim 13 and Eddington et al. (US 5,165,017) as applied above to claim 13 in view of the AAPA (Figures 1A and 1B) as applied above to claim 13 in further view of Tanikawa et al. (US 2002/0048193).

Regarding claim 17, Lavaud as modified by Eddington and AAPA fails to disclose that the register is a pulse width register having five bits. Tanikawa discloses a register the controls a pulse width (page 7, paragraph 0083; reads on pulse width register). The examiner takes official notice that the bit size of a register is known to be variable depending upon how many bits the designer want it to have. It would have been obvious to modify Lavaud as modified by Eddington and AAPA so that the register is a pulse width register in order to provide better control over the device.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Devona E. Faulk whose telephone number is 571-272-7515. The examiner can normally be reached on 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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